ABSTRACT OF THE DISCLOSURE

An apparatus for detecting storehit conditions and forwarding storehit data within microprocessor pipeline stages is provided. The apparatus has a result forwarding cache (RFC) that holds a predetermined number of store instruction results corresponding to stages near the end of the pipeline and a plurality of store buffers that hold store instruction results waiting to be written to a data cache. A set of address comparators associated with each of the RFC and store buffers compares a load address of a load instruction executed subsequent to the store instructions, and detects matches of the load address with store addresses of the various store instruction results in the RFC and store buffers. Control logic receives the comparison information and forwards the newest matching data in the pipeline, either from the RFC or store buffers, accordingly. The RFC comparators compare virtual addresses and the store buffer comparators compare physical addresses for improved timing. The data is speculatively forwarded based on the virtual address comparisons and in some instances the speculatively forwarded data must be corrected if a virtual alias condition occurs or if the load address was in a non-cacheable region of the microprocessor address space.